CLAIMS

What is claimed is:

1. An ESD-protection structure, comprising:

an integrated circuit having a lighter doped p-silicon well (P- well);

a first lighter doped n-silicon well (first N- well) in the P- well;

a plurality of first heavier doped p-silicon diffusions (first P+ diffusions) in the first N- well;

a first heavier doped n-silicon diffusion (first N+ diffusion) in the first N- well, wherein the first N+ diffusion surrounds the plurality of first P+ diffusions;

a second lighter doped n-silicon well (second N- well) in the P- well, the second N- well adjacent to the first N- well;

a second heavier doped n-silicon diffusion (second N+ diffusion) in the second N- well, the second N+ diffusion is connected to the first N+ diffusion;

a second heavier doped p-silicon diffusion (second P+ diffusion) in the second N- well;

a third heavier doped p-silicon diffusion (third P+ diffusion) in the P- well, the third P+ diffusion is connected to the second P+ diffusion, wherein the third P+ diffusion surrounds the first N+ diffusion, the plurality of first P+ diffusions, the second N+ diffusion and the second P+ diffusion;

a bond pad connected to the plurality of first P+ diffusions; and

a connection to the third N+ diffusion.

2. The ESD-protection structure of claim 1, wherein the P- well is the integrated circuit substrate.

3. The ESD-protection structure of claim 1, further comprising a lighter doped n-silicon substrate (N- substrate) of the integrated circuit, wherein the P- well is in the N- substrate.

4. The ESD-protection structure of claim 1, wherein the plurality of first P+ diffusions are rectangular shaped.

5. The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions are square shaped.

6. The ESD-protection structure of claim 1, wherein the plurality of P+ diffusions are stripe shaped.

7. The ESD-protection structure of claim 1, wherein the bond pad is connected to the plurality of first P+ diffusions with a first plurality of conductive vias.

8. The ESD-protection structure of claim 1, wherein the connection between the first and second N+ diffusions is with a second plurality of conductive vias.

9. The ESD-protection structure of claim 1, wherein the connection between the second and third P+ diffusions is with a third plurality of conductive vias.

10. The ESD-protection structure of claim 7, wherein the first plurality of conductive vias are metal.

11. The ESD-protection structure of claim 7, wherein the first plurality of conductive vias comprise conductive semiconductor silicon.

12. The ESD-protection structure of claim 8, wherein the second plurality of conductive vias are metal.

13. The ESD-protection structure of claim 8, wherein the second plurality of conductive vias comprise conductive silicon.

14. The ESD-protection structure of claim 9, wherein the third plurality of conductive vias are metal.

15. The ESD-protection structure of claim 9, wherein the third plurality of conductive vias comprise conductive silicon.

16. The ESD-protection structure of claim 1, further comprising a second connection to the first N+ diffusion with a fourth plurality of conductive vias.

17. The ESD-protection structure of claim 1, wherein the P- well is coupled to ground.

18. The ESD-protection structure of claim 1, wherein the P- well is coupled to a common power supply rail.

19. The ESD-protection structure of claim 1, wherein the third P+ diffusion is coupled to ground.

20. The ESD-protection structure of claim 1, wherein the third P+ diffusion is coupled to a common power supply rail.

21. The ESD-protection structure of claim 1, wherein the plurality of first P+ diffusions are located substantially under the bond pad.

22. A system for protecting an integrated circuit from ESD damage, said system comprising:

an ESD-protection structure for at least one of a plurality of input and output connections of an integrated circuit, wherein the ESD-protection structure comprises:

an integrated circuit having a lighter doped p-silicon well (P- well);

a first lighter doped n-silicon well (first N- well) in the P- well;

a plurality of first heavier doped p-silicon diffusions (first P+ diffusions) in the first N- well;

a first heavier doped n-silicon diffusion (first N+ diffusion) in the first N- well, wherein the first N+ diffusion surrounds the plurality of first P+ diffusions;

a second lighter doped n-silicon well (second N- well) in the P- well, the second N- well adjacent to the first N- well;

a second heavier doped n-silicon diffusion (second N+ diffusion) in the second N- well, the second N+ diffusion is connected to the first N+ diffusion;

a second heavier doped p-silicon well (second P+ diffusion) in the second N- well;

a third heavier doped p-silicon diffusion (third P+ diffusion) in the P- well, the third P+ diffusion is connected to the second P+ diffusion, wherein the third P+ diffusion surrounds the first N+ diffusion, the plurality of first P+ diffusions, the second N+ diffusion and the second P+ diffusion;

a bond pad connected to the plurality of first P+ diffusions; and

a connection to the third N+ diffusion.

23. An ESD-protection structure, comprising:

a PNP transistor structure comprising a base, collector and emitter, wherein the emitter is coupled to an integrated circuit pad and the collector is coupled to a common; and

a trigger device having a controlled breakdown voltage is coupled to the base of the PNP transistor structure, wherein the PNP transistor structure conducts between the pad and the common when the controlled breakdown voltage of the trigger device is exceeded and the PNP transistor structure does not conduct otherwise.

24. The ESD-protection structure of claim 23, wherein the common is coupled to a common supply voltage.

25. The ESD-protection structure of claim 23, wherein the common is coupled to ground.

26. The ESD-protection structure of claim 23, wherein the trigger device is a diode.

27. The ESD-protection structure of claim 23, wherein the controlled breakdown voltage of the trigger device is less than a destructive breakdown voltage of an integrated circuit transistor connected to the pad.

28. The ESD-protection structure of claim 23, wherein the PNP transistor structure conducts substantially all of the current from an ESD event.

29. The ESD-protection structure of claim 23, wherein the PNP transistor structure is substantially under the pad.

30. The ESD-protection structure of claim 23, wherein the trigger device is substantially under the pad.

31. A method of protecting an integrated circuit pad from an ESD event, said method comprising the steps of:

connecting a PNP transistor structure comprising a base, collector and emitter, wherein the emitter is coupled to an integrated circuit pad and the collector is coupled to a common; and

connecting a trigger device having a controlled breakdown voltage to the base of the PNP transistor structure such that the trigger device controls

conduction of the PNP transistor structure, wherein when an ESD event occurs having a voltage greater than the controlled breakdown voltage of the trigger device, the PNP transistor structure is substantially conductive between the pad and the common and is substantially non-conductive otherwise.